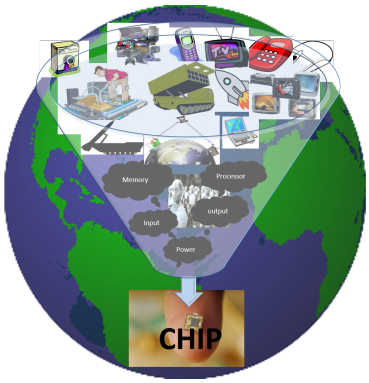
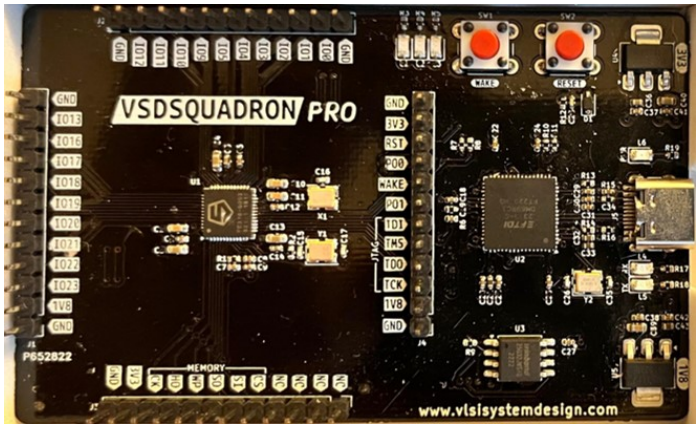


VLSI System Design (VSD)

VSDSquadron PRO

powered by SiFive

Step into the future with the VSDSquadron PRO board, powered by SiFive - where RISC-V ISA meets education, providing a dynamic sandbox for hands-on innovation in AI, ML, IoT, and edge computing



Contents

List of Tables

List of Figures

1 Getting Started

The VSDSquadron PRO RISC-V development board - Features and specifications:

- **Tailored for IoT and Edge Computing**: The FE310-G002 is designed with students in mind, offering an ideal platform to explore IoT and edge computing applications
- **High-Performance CPU Core**: Powered by the SiFive Essential^{TM} E3 Series CPU Core Complex, featuring a 32-bit RV32IMAC core, students can dive into real-world performance while learning RISC-V architecture
- **Memory for Enhanced Learning**: With a 16KB L1 Instruction Cache and a 16KB Data SRAM scratchpad, the board allows students to experiment with data processing and efficient instruction handling
- **Hardware Multiply/Divide**: Equipped with hardware multiply and divide capabilities, it helps students grasp essential computational functions for advanced projects
- **RISC-V Debugging Made Simple**: The debug module, fully compatible with the RISC-V debug spec 0.13, simplifies the debugging process, making it easier for students to identify and fix issues in real-time
- **Flexible Clock Generation**: On-chip oscillators and PLLs provide flexible clock generation, giving students practical experience with system timing and frequency control
- **Diverse Peripheral Support**: The FE310 offers a rich set of peripherals, including UARTs, I2C, QSPI, PWMs, and timers, enabling students to connect various external devices and expand project possibilities
- **Power Efficiency**: With multiple power domains and a low-power standby mode, the board is optimized for hands-on student projects that require energy-efficient solutions
- **Versatile Applications**: Whether for building IoT devices, exploring machine learning at the edge, or developing low-power embedded systems, the FE310 provides a robust platform for learning and experimentation

The VSDSquadron PRO board, powered by the FE310-G002 chip, is designed for IoT and edge computing. It features a 32-bit RV32IMAC core, 16KB L1 cache, and Data SRAM, along with flexible clock generation and multiple peripherals. With hardware multiply/divide functions and a RISC-V compatible debug module, it supports energy-efficient, low-power standby modes, making it ideal for a variety of applications.

1.1 Kit Contents

The following table number 1 lists the contents of the VSDSquadron PRO RISC-V development board.

Item	Quantity
VSDSquadron PRO RISC-V development board featuring the 32-bit RISC-V core FE310-G002, from SiFive, based on RV32IMAC instruction set	1

Table 1: Kit Contents

1.2 Block Diagram

The block diagram shown in Figure 1 shows the key components of the VSDSquadron PRO RISC-V development board.

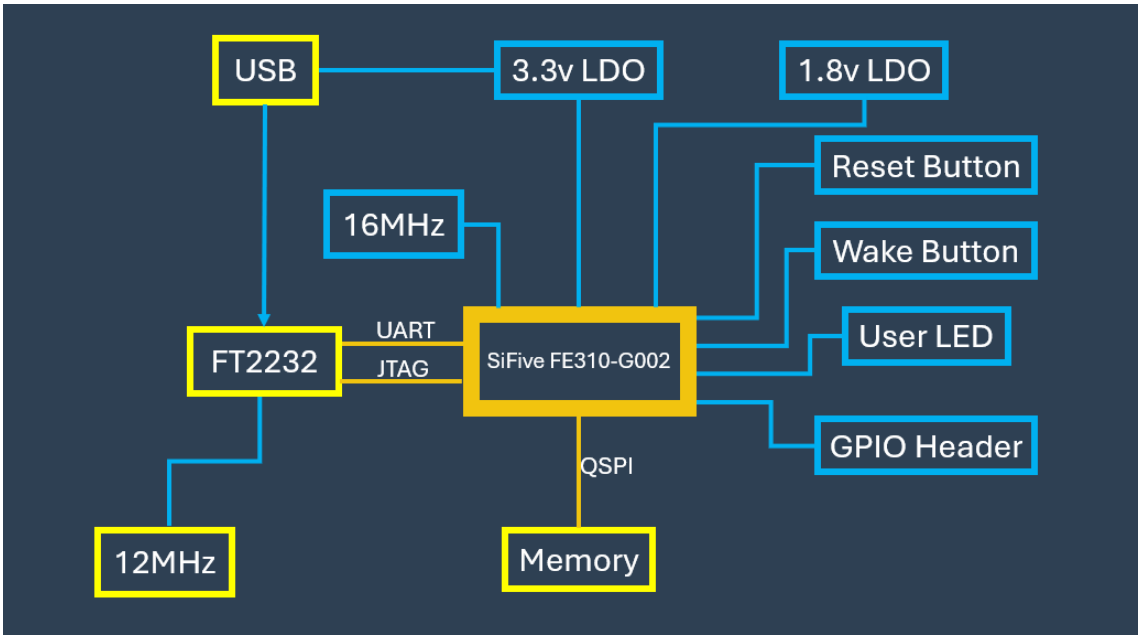


Figure 1: VSDSquadron PRO RISC-V development board Block Diagram

1.3 Web Resources

For more information about the VSDSquadron PRO RISC-V SoC device, refer to FE310-G002 RISC-V SoC Datasheet and FE310-G002 Manual

1.4 Board Overview

The VSDSquadron PRO RISC-V development boards features a RISC-V SoC with the following capabilities:

- 48-lead 6x6 QFN package

- On-board 16MHz crystal
- 19 Digital IO pins and 9 PWM pins
- 2 UART and 1 I2C
- Dedicated quad-SPI (QSPI) flash interface
- 32 Mbit Off-Chip (ISSI SPI Flash)
- USB-C type for Program, Debug, and Serial Communication

The following illustration in Figure 2 highlights various components of the VSDSquadron PRO RISC-V development board.

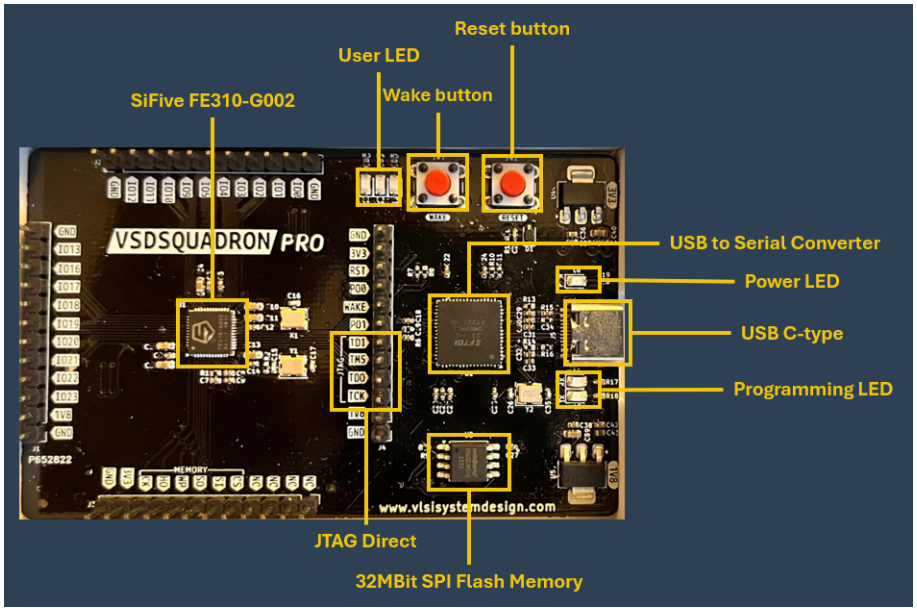


Figure 2: VSDSquadron PRO RISC-V development board

1.4.1 Form Factor

The following are the dimensions of the VSDSquadron PRO RISC-V development board.

- Form factor is 84.00 x 52.00 mm
- Maximum height of the component at the top side: 8mm
- Maximum height of the component at the bottom side: 1mm

1.4.2 Table 2 shows FE310-G002 RISC-V SoC IO Bank Assignment for communication Interfaces

Pin Name	GPIO	PWM	SPI	UART	I2C
IO0	0 I/O	PWM0_0 O			
IO1	1 I/O	PWM0_1 O			
IO2	2 I/O	PWM0_2 O	SPI1_SS0		
IO3	3 I/O	PWM0_3 O	SPI1_MOSI		
IO4	4 I/O		SPI1_MISO		
IO5	5 I/O		SPI1_SCK		
IO9	9 I/O		SPI1_SS2		
IO10	10 I/O	PWM2_0 O	SPI1_SS3		
IO11	11 I/O	PWM2_1 O			
IO12	12 I/O	PWM2_2 O			I2C0_SDA
IO13	13 I/O	PWM2_3 O			I2C0_SCL
IO16	16 I/O			UART0_RX I	
IO17	17 I/O			UART0_TX O	
IO18	18 I/O			UART1_TX O	
IO19	19 I/O	PWM1_1 O			
IO20	20 I/O	PWM1_0 O			
IO21	21 I/O	PWM1_2 O			
IO22	22 I/O	PWM1_3 O			
IO23	23 I/O			UART1_RX I	

Table 2: FE310-G002 RISC-V SoC IO Bank Assignment

1.4.3 The following table 3 lists the important components of the VSDSquadron PRO RISC-V development board

Board	VSDSquadron PRO
Microcontroller	FE310-G002 chip with 32-bit RISC-V core based on RV32IMAC instruction set
USB connector	USB 2.0 Type-C
Built-in LED Pin	GPIO 19, 21, 22
Digital I/O pins	19
Analog I/O pins	The FE310-G002 has an I^2C controller to communicate with external I^2C devices, such as sensors, ADCs, etc.
PWM pins	9
External interrupt pins	19
External Wakeup pins	1
UART	2, IO16 and IO17 (RX0 and TX0), IO23 and IO18(RX1 and TX1)
I2C	1, IO12(SDA), IO13(SCL)
SPI Controllers/HW CS Pins	1/3, IO5(SCK), IO2(SS0), IO3(MOSI), IO4(MISO), IO9(SS2), IO10(SS3)
I/O voltage	3.3V
Input voltage (nominal)	5V
Clock speed	Processor: 320MHz
Flash Memory	32 Mbit Off-Chip (ISSI SPI Flash)

Table 3: Specifications of the VSDSquadron PRO Board

1.5 Handling the Board

To avoid causing any damage or malfunctions, it is important to be mindful of the following points when handling or operating the board:

- To prevent any damage, make sure to handle the board while taking electrostatic discharge (ESD) precautions.
- Power down the board by disconnecting the board from USB port

1.6 Operating Temperature

Designed for Room Temperature. The standard range for room temperature in Celsius is typically considered to be between 20 to 35 degrees Celsius (or 68 to 95 degrees Fahrenheit).

1.7 Powering Up the Board

Connect the Type-C end of USB cable to the board as shown in below image and refer to Installation and Settings for programming the board. Do this step after software installation, which is a time-consuming process

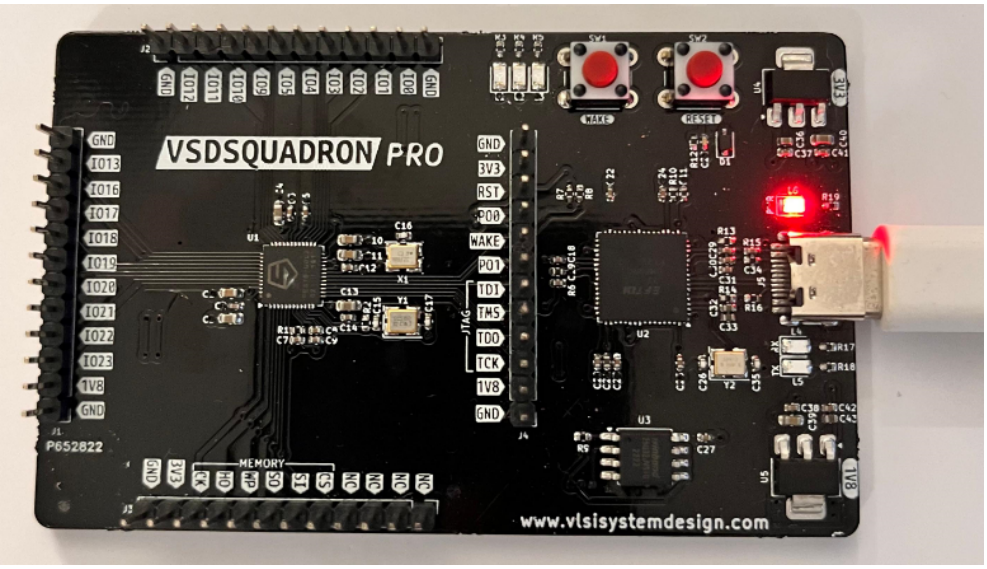


Figure 3: Micro-C end of USB cable connected to board

2 Installation and Settings

This section provides information about the software and hardware settings required to run "sifive-welcome" on the VSDSquadron PRO RISC-V development board using Freedom Studio

2.1 Download drivers

- Download Zadig from https://zadig.akeo.ie/
- Open Zadig from the location of the folder where you downloaded it. Click on "Options" tab and select "List All Devices". Then select "Dual RS-232-HS (Interface 0) as represented by 2 in Figure 4. Choose "libusb-win32" software as represented by 3 in Figure 4. Finally click on "Install or Reinstall Driver" as represented by 4 in same Figure 4.

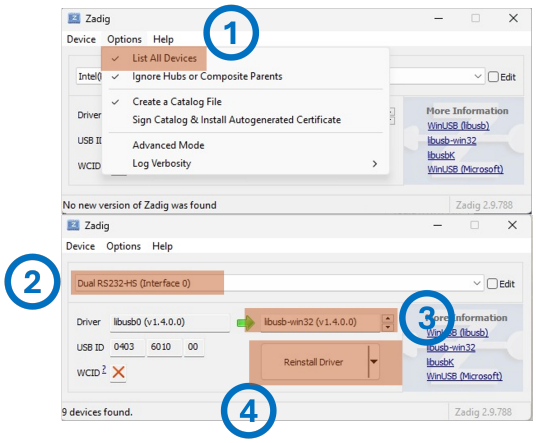


Figure 4: Steps to install driver using Zadig

2.2 Extract Freedom Studio from VSDSquadronPRO Tar GZ file

- Download Freedom Studio, preferably on the D: drive or C: drive, from https://forgefunder.com/ kunal/VSDSquadronPRO.tar.gz.
- Right click on VSDSquadronPRO.tar and click on "Extract All", as shown in Figure 5.
- Select the destination folder and click on "Extract".

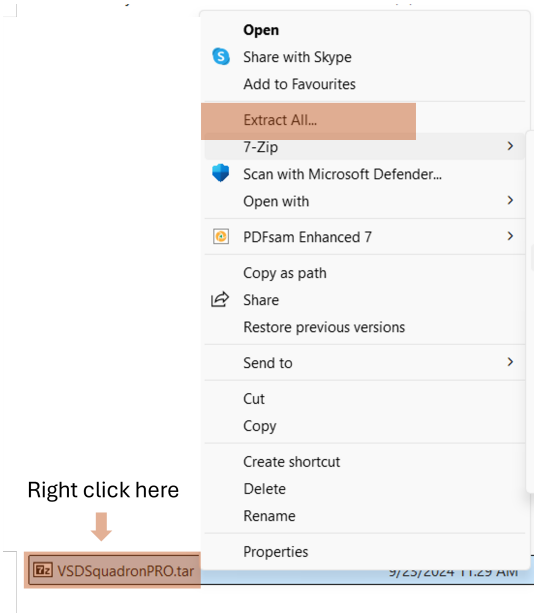


Figure 5: Freedom Studio Extraction step from VSDSquadronPRO.tar.gz

2.3 Run example "sifive-welcome" program on VSDSquadron PRO board

- Go to folder highligted in Figure 6 and you should see all required files as shown in same Figure 6

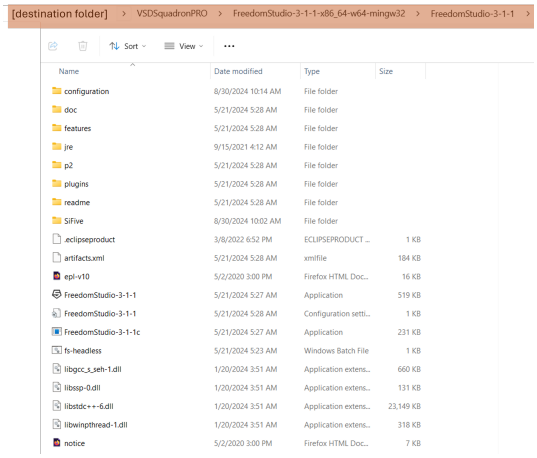


Figure 6: Freedom Studio 3.1.1 extracted folder structure

- Double Click on "FreedomStudio-3-1-1" represented as 1 in Figure 7. In case you get the green box which is represented as 2 in the same Figure 7, click on "More Info" and then click on "Run anyway". After that, you would see the "FreedomStudio" software launched as shown in same Figure 7 represented by 3

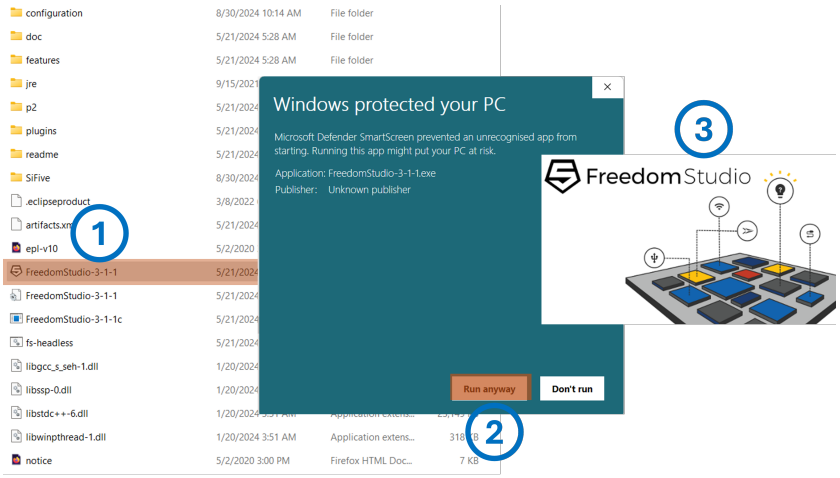


Figure 7: FreedomStudio GUI launch in 3 steps

- Create and select a directory as workspace, then click on "Launch" button as shown in Figure 8:

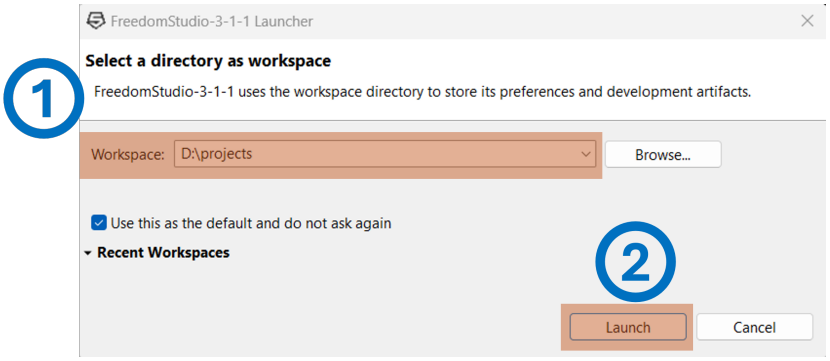


Figure 8: Workspace Creation

- Create a new Validation Software Project. Select the SDK, sifive-hifive1 target, example and Create a debug launch config as shown in Figure 9

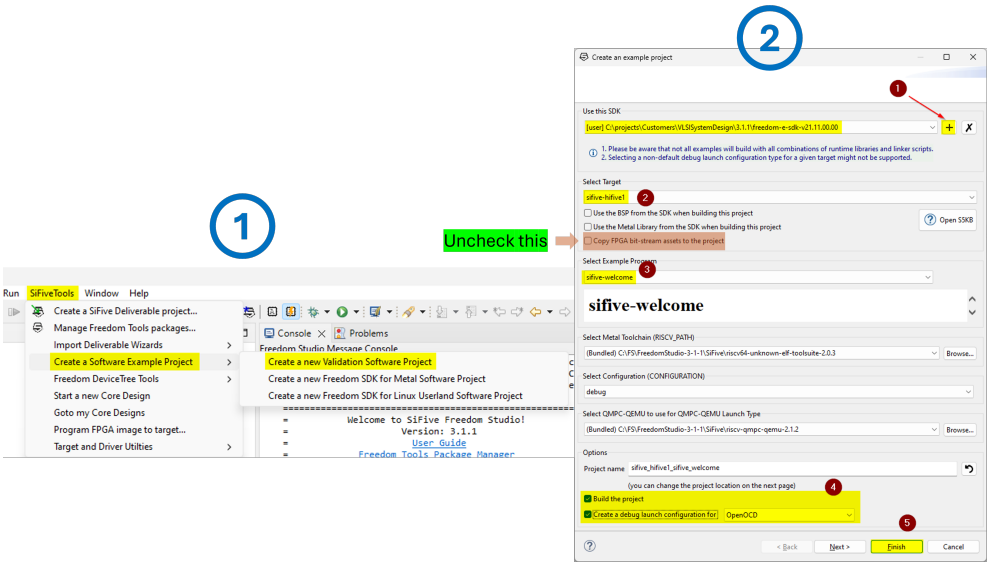


Figure 9: Create New Software Project

- Once you click the "Debug" button from above step, you would see the "Debug Configuration" window. Connect VSDSquadron PRO board to your laptop, click on "OpenOCD" tab and then click on "Debug". See Figure 10 for more details

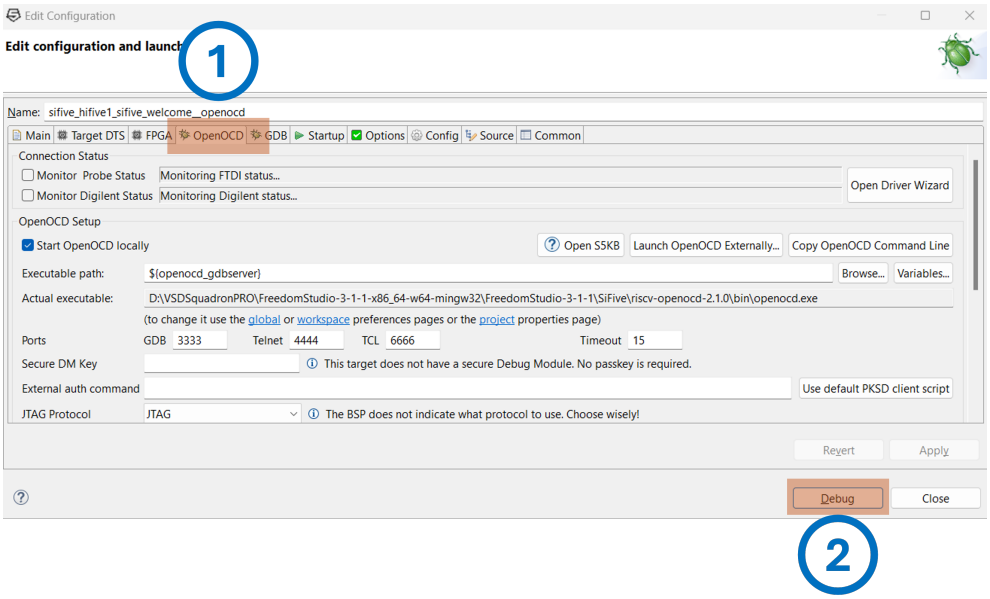


Figure 10: Steps to open debug session using OpenOCD

- **Optional** - If you don't see the "Debug Configuration" window by default OR if you want

to run another debug session, the click on Debug button as shown in Figure 11 and click on "Debug Confgurations". Then click on "OpenOCD" tab and hit the "Debug" button. Refer to Figure 11 for more details

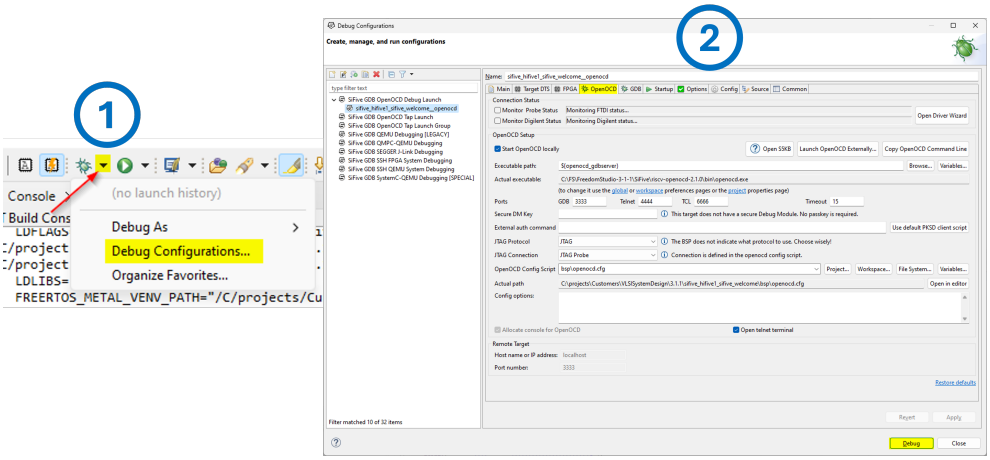


Figure 11: Alternate method to open debug session using OpenOCD

- You should see the debug window shown with 1 shown in Figure 12. To run the program, click on the "Run" button as represented by 2 in the same Figure 12

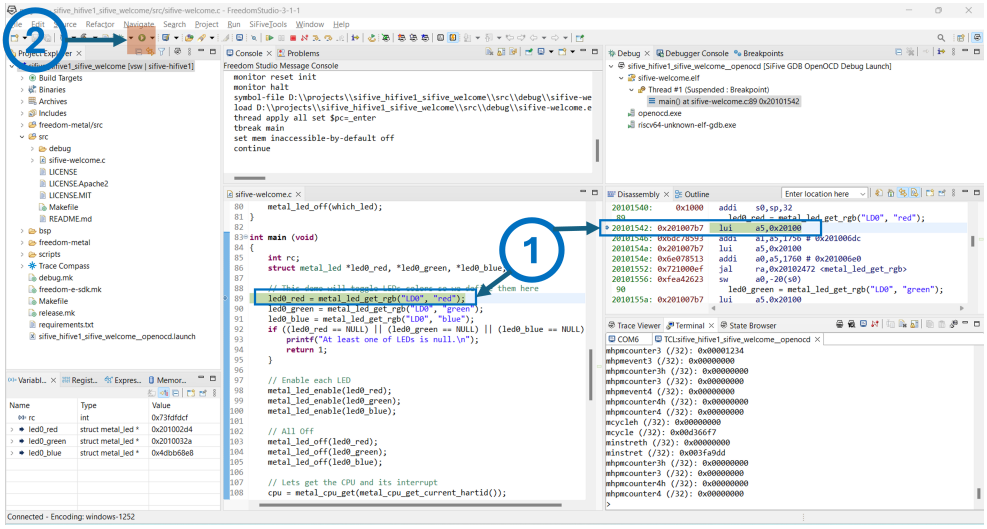


Figure 12: Steps to run sifive-welcome program and observe output

- If you see a message "You have an active OpenOCD debug launch. Would you like to terminate that one and continue this one?" as shown in Figure 13, click on "Yes". Finally, you would see "SiFive" as output in the Com terminal represented by 2 in same Figure 13. The blue LED on VSDSquadron PRO should blink after this step.

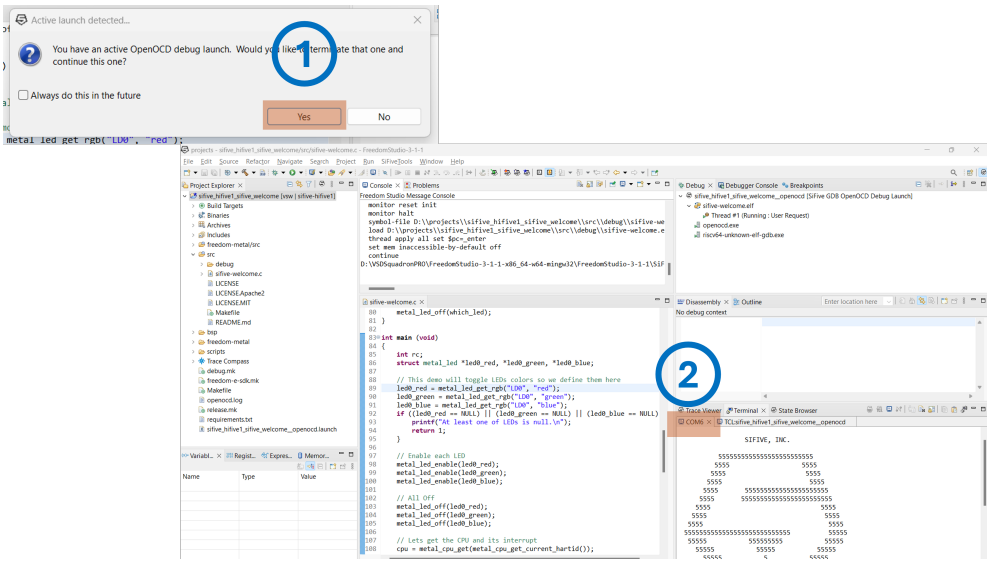


Figure 13: Run program and see output

3 Board Component Placement

The following figure shows the placement of various components on the VSDSquadron PRO RISC-V development board.

3.1 VSDSquadron PRO top view

The following Figure 14 shows the top view of the VSDSquadron PRO RISC-V development board.

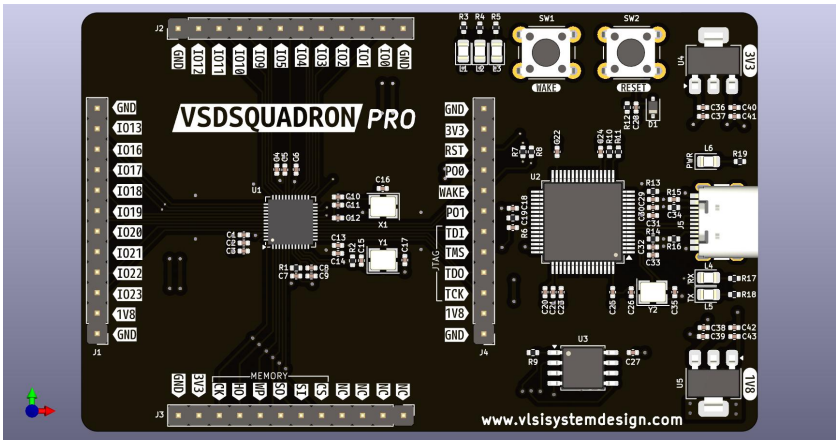


Figure 14: Silkscreen Top View

3.2 VSDSquadron PRO bottom view

The following Figure 15 shows the bottom view of the VSDSquadron PRO RISC-V development board silkscreen.

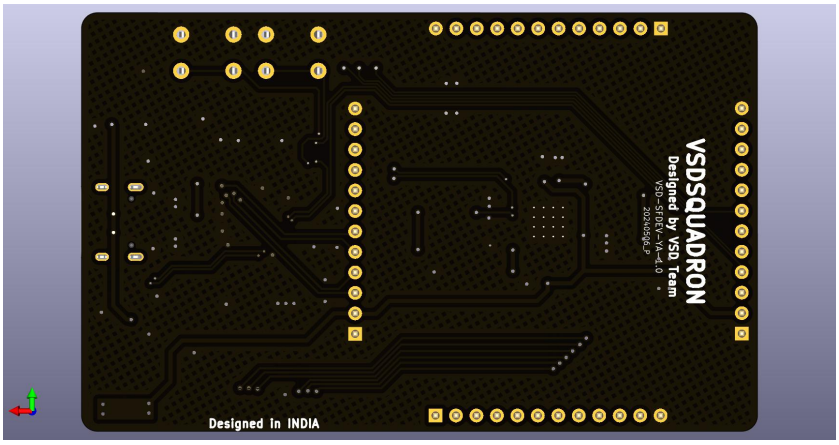


Figure 15: Silkscreen Top View

4 Revision History

The document's revision history provides a record of the alterations made to it, listed in chronological order, with the most recent revision first.

Revision	Date	Description
1.0	-	This is the first publication of this document

Table 4: Revision History

5 Help and support

- Contact email ID - vsd@vlsisystemdesign.com
- Online Slack support - https://vsdsquadron.slack.com/