

VLSI System Design (VSD)

VSDSquadron **PRO**

powered by SiFive

Step into the future with the VSDSquadron PRO board, powered by SiFive - where RISC-V ISA meets education, providing a dynamic sandbox for hands-on innovation in AI, ML, IoT, and edge computing



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1 Getting Started

The VSDSquadron PRO RISC-V development board - Features and specifications:

- **Tailored for IoT and Edge Computing**: The FE310-G002 is designed with students in mind, offering an ideal platform to explore IoT and edge computing applications
- High-Performance CPU Core: Powered by the SiFive EssentialTM E3 Series CPU Core Complex, featuring a 32-bit RV32IMAC core, students can dive into real-world performance while learning RISC-V architecture
- Memory for Enhanced Learning: With a 16KB L1 Instruction Cache and a 16KB Data SRAM scratchpad, the board allows students to experiment with data processing and efficient instruction handling
- Hardware Multiply/Divide: Equipped with hardware multiply and divide capabilities, it helps students grasp essential computational functions for advanced projects
- **RISC-V Debugging Made Simple**: The debug module, fully compatible with the RISC-V debug spec 0.13, simplifies the debugging process, making it easier for students to identify and fix issues in real-time
- Flexible Clock Generation: On-chip oscillators and PLLs provide flexible clock generation, giving students practical experience with system timing and frequency control
- Diverse Peripheral Support: The FE310 offers a rich set of peripherals, including UARTs, I2C, QSPI, PWMs, and timers, enabling students to connect various external devices and expand project possibilities
- **Power Efficiency**: With multiple power domains and a low-power standby mode, the board is optimized for hands-on student projects that require energy-efficient solutions
- Versatile Applications: Whether for building IoT devices, exploring machine learning at the edge, or developing low-power embedded systems, the FE310 provides a robust platform for learning and experimentation

The VSDS quadron PRO board, powered by the FE310-G002 chip, is designed for IoT and edge computing. It features a 32-bit RV32IMAC core, 16KB L1 cache, and Data SRAM, along with flexible clock generation and multiple peripherals. With hardware multiply/divide functions and a RISC-V compatible debug module, it supports energy-efficient, low-power standby modes, making it ideal for a variety of applications.

1.1 Kit Contents

The following table number 1 lists the contents of the VSDS quadron PRO RISC-V development board.

Item	Quantity
VSDSquadron PRO RISC-V development board featuring the 32- bit RISC-V core FE310-G002, from SiFive, based on RV32IMAC instruction set	1

Table 1: Kit Contents

1.2 Block Diagram

The block diagram shown in Figure 1 shows the key components of the VSDS quadron PRO RISC-V development board.



Figure 1: VSDSquadron PRO RISC-V development board Block Diagram

1.3 Web Resources

For more information about the VSDS quadron PRO RISC-V SoC device, refer to FE310-G002 RISC-V SoC Data sheet and FE310-G002 Manual

1.4 Board Overview

The VSDS quadron PRO RISC-V development boards features a RISC-V SoC with the following capabilities:

• 48-lead 6x6 QFN package

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User Guide

- On-board 16MHz crystal
- 19 Digital IO pins and 9 PWM pins
- 2 UART and 1 I2C
- Dedicated quad-SPI (QSPI) flash interface
- 32 Mbit Off-Chip (ISSI SPI Flash)
- USB-C type for Program, Debug, and Serial Communication

The following illustration in Figure 2 highlights various components of the VSDS quadron PRO RISC-V development board.



Figure 2: VSDSquadron PRO RISC-V development board

1.4.1 Form Factor

The following are the dimensions of the VSDSquadron PRO RISC-V development board.

- $\bullet\,$ Form factor is 84.00 x 52.00 mm
- Maximum height of the component at the top side: 8mm
- Maximum height of the component at the bottom side: 1mm

Pin	GPIO	PWM	SPI	UART	I2C
Name					
IO0	0 I/O	PWM0_0 O			
IO1	1 I/O	PWM0_1 O			
IO2	2 I/O	PWM0_2 O	SPI1_SS0		
IO3	3 I/O	PWM0_3 O	SPI1_MOSI		
IO4	4 I/O		SPI1_MISO		
IO5	5 I/O		SPI1_SCK		
IO9	9 I/O		SPI1_SS2		
IO10	10 I/O	PWM2_0 O	SPI1_SS3		
IO11	11 I/O	PWM2_1 O			
IO12	12 I/O	PWM2_2 O			I2C0_SDA
IO13	13 I/O	PWM2_3 O			I2C0_SCL
IO16	16 I/O			UART0_RX I	
IO17	17 I/O			UART0_TX O	
IO18	18 I/O			UART1_TX O	
IO19	19 I/O	PWM1_1 O			
IO20	20 I/O	PWM1_0 O			
IO21	21 I/O	PWM1_2 O			
IO22	22 I/O	PWM1_3 O			
IO23	23 I/O			UART1_RX I	

1.4.2 Table 2 shows FE310-G002 RISC-V SoC IO Bank Assignment for communication Interfaces

Table 2: FE310-G002 RISC-V SoC IO Bank Assignment

Board	VSDSquadron PBO
Microcontrollor	FE310 C002 chip with 32 bit PISC V
Microcontroner	FESTO-GOUZ CIIIP WITH 52-DIT RISC-V
	core based on RV32IMAC instruction set
USB connector	USB 2.0 Type-C
Built-in LED Pin	GPIO 19, 21, 22
Digital I/O pins	19
Analog I/O pins	The FE310-G002 has an I ² C controller to
	communicate with external I ² C devices,
	such as sensors, ADCs, etc.
PWM pins	9
External interrupt pins	19
External Wakeup pins	1
UART	2, IO16 and IO17 (RX0 and TX0), IO23
	and IO18(RX1 and TX1)
I2C	1, IO12(SDA), IO13(SCL)
SPI Controllers/HW CS Pins	1/3, IO5(SCK), IO2(SS0), IO3(MOSI),
	IO4(MISO), IO9(SS2), IO10(SS3)
I/O voltage	3.3V
Input voltage (nominal)	5V
Clock speed	Processor: 320MHz
Flash Memory	32 Mbit Off-Chip (ISSI SPI Flash)

1.4.3 The following table 3 lists the important components of the VSDSquadron PRO RISC-V development board

Table 3: Specifications of the VSDSquadron PRO Board

1.5 Handling the Board

To avoid causing any damage or malfunctions, it is important to be mindful of the following points when handling or operating the board:

- To prevent any damage, make sure to handle the board while taking electrostatic discharge (ESD) precautions.
- Power down the board by disconnecting the board from USB port

1.6 Operating Temperature

Designed for Room Temperature. The standard range for room temperature in Celsius is typically considered to be between 20 to 35 degrees Celsius (or 68 to 95 degrees Fahrenheit).

1.7 Powering Up the Board

Connect the Type-C end of USB cable to the board as shown in below image and refer to Installation and Settings for programming the board. Do this step after software installation, which is a time-consuming process



Figure 3: Micro-C end of USB cable connected to board

2 Installation and Settings

This section provides information about the software and hardware settings required to run "sifive-welcome" on the VSDSquadron PRO RISC-V development board using Freedom Studio

2.1 Download drivers

- Download Zadig from https://zadig.akeo.ie/
- Open Zadig from the location of the folder where you downloaded it. Click on "Options" tab and select "List All Devices". Then select "Dual RS-232-HS (Interface 0) as represented by 2 in Figure 4. Choose "libusb-win32" software as represented by 3 in Figure 4. Finally click on "Install or Reinstall Driver" as represented by 4 in same Figure 4.



Figure 4: Steps to install driver using Zadig

2.2 Extract Freedom Studio from VSDSquadronPRO Tar GZ file

- Download Freedom Studio, preferably on the D: drive or C: drive, from https://forgefunder.com/ ku-nal/VSDSquadronPRO.tar.gz.
- Right click on VSDSquadronPRO.tar and click on "Extract All", as shown in Figure 5.
- Select the destination folder and click on "Extract".



Figure 5: Freedom Studio Extraction step from VSDSquadronPRO.tar.gz

2.3 Run example "sifive-welcome" program on VSDSquadron PRO board

- Go to folder highligted in Figure 6 and you should see all required files as shown in same Figure $_6$

ation folder] > VSDSquadronPRO	> FreedomStudio-	3-1-1-x86_64-w64-r	ningw32 >	FreedomStudio-3-1-1	>
② ③ ↑↓ Sort ~ ■ View ~					
Name	Date modified	Туре	Size		
tonfiguration	8/30/2024 10:14 AM	File folder			
📁 doc	5/21/2024 5:28 AM	File folder			
ieatures	5/21/2024 5:28 AM	File folder			
📁 jre	9/15/2021 4:12 AM	File folder			
🚞 p2	5/21/2024 5:28 AM	File folder			
📁 plugins	5/21/2024 5:28 AM	File folder			
🚞 readme	5/21/2024 5:28 AM	File folder			
SiFive	8/30/2024 10:02 AM	File folder			
eclipseproduct	3/8/2022 6:52 PM	ECLIPSEPRODUCT	1 KB		
artifacts.xml	5/21/2024 5:28 AM	xmlfile	184 KB		
epl-v10	5/2/2020 3:00 PM	Firefox HTML Doc	16 KB		
FreedomStudio-3-1-1	5/21/2024 5:27 AM	Application	519 KB		
FreedomStudio-3-1-1	5/21/2024 5:28 AM	Configuration setti	1 KB		
FreedomStudio-3-1-1c	5/21/2024 5:27 AM	Application	231 KB		
🖫 fs-headless	5/21/2024 5:23 AM	Windows Batch File	1 KB		
libgcc_s_seh-1.dll	1/20/2024 3:51 AM	Application extens	660 KB		
libssp-0.dll	1/20/2024 3:51 AM	Application extens	131 KB		
libstdc++-6.dll	1/20/2024 3:51 AM	Application extens	23,149 KB		
libwinpthread-1.dll	1/20/2024 3:51 AM	Application extens	318 KB		
notice	5/2/2020 3:00 PM	Firefox HTML Doc	7 KB		

Figure 6: Freedom Studio 3.1.1 extracted folder structure

• Double Click on "FreedomStudio-3-1-1" represented as 1 in Figure 7. In case you get the green box which is represented as 2 in the same Figure 7, click on "More Info" and then click on "Run anyway". After that, you would see the "FreedomStudio" software launched as shown in same Figure 7 represented by 3

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Figure 7: FreedomStudio GUI launch in 3 steps

• Create and select a directory as workspace, then click on "Launch" button as shown in Figure 8:

	₿ Freedoms	Studio-3-1-1 Launcher	×
1	Select a dir FreedomStu	ectory as workspace dio-3-1-1 uses the workspace directory to store its preferences and development artifacts.	
	Workspace:	D\projects V Browse	
	 ✓ Use this a ✓ Recent Wo 	s the default and do not ask again rkspaces Launch Cancel	

Figure 8: Workspace Creation

• Create a new Validation Software Project. Select the SDK, sifive-hifive1 target, example and Create a debug launch config as shown in Figure 9



Figure 9: Create New Software Project

• Once you click the "Debug" button from above step, you would see the "Debug Configuration" window. Connect VSDSquadron PRO board to your laptop, click on "OpenOCD" tab and then click on "Debug". See Figure 10 for more details

Edit Configuration		— D
dit configuration an	nd launct	×
ame: sifive_hifive1_sifi	ive_welcome_openocd	
🗎 Main 🗱 Target DTS	幕 FPGA 🏂 OpenOCD 🏂 GDB 🕨 Startup 🗹 Options ⊚ 0	nfig 🦻 Source 🔲 Common
Connection Status		
Monitor Probe Star	tus Monitoring FTDI status	Open Driver Wizard
Monitor Digilent St	tatus Monitoring Digilent status	
OpenOCD Setup		
Start OpenOCD loc	ally	Open S5KB Launch OpenOCD Externally Copy OpenOCD Command Line
Executable path:	\${openocd_gdbserver}	Browse Variables
Actual executable:	D:\VSDSquadronPRO\FreedomStudio-3-1-1-x86_64-w64	mingw32\FreedomStudio-3-1-1\SiFive\riscv-openocd-2.1.0\bin\openocd.exe
	(to change it use the global or workspace preferences page	es or the <u>project</u> properties page)
Ports	GDB 3333 Telnet 4444 TCL 6666	Timeout 15
Secure DM Key	 This target does not 	ve a secure Debug Module. No passkey is required.
External auth comman	nd	Use default PKSD client script
JTAG Protocol	JTAG V (1) The BSP does not inc	ate what protocol to use. Choose wisely!
		Reyert Apply
?		Debug Close
		(2)

Figure 10: Steps to open debug session using OpenOCD

• Optional - If you don't see the "Debug Configuration" window by default OR if you want

to run another debug session, the click on Debug button as shown in Figure 11 and click on "Debug Confgurations". Then click on "OpenOCD" tab and hit the "Debug" button. Refer to Figure 11 for more details

		Debug Configurations			C		- 0
		Create, manage, and run con	figurations		(2	:)	1
				Name silve_hilvel_silve_m	dcome_operocd		
		type filter text		Main 😫 Target DTS 😫	FPGA 🕸 OpenOCD 🕸 GDB 🔛 Startup 🜄 Options 🔅	Config Source Common	
(1)	 G SFive 608 OpenOCD Del Sfive 000000 Jake Sfive 008 OpenOCD Tap SFive 608 OpenOCD Ta	rug Launch scome_openocd Launch Launch Group ging [LEGACY] Debugging	Connection Status Monitor Probe Status Monitor Digilent Status OpenOCD Setup	Monitoring FTDI status Monitoring Digilent status		Open Driver Wizard
1 mm (mm) + + +		SIFive GDB SEGGER J-Link	Debugging	Start OpenOCD locally		(2) Open SSKB Launch OpenOCD External	Copy OpenOCD Command Line
🛛 🔂 🚸	<mark>-</mark> 🜔 - 🗐 - 🎦 🔗 - 🟒	BY SIFINE GDB SSH EPGA Sys BY SIFINE GDB SSH QEMU Sy	.em Debugging stem Debugging	Executable path:	(openocd_gdbserver)		Browse Variables
· · · · · · · · · · · · · · · · · · ·		SiFive GDB SystemC-QEN	4J Debugging [SPECIAL]	Actual executables	://FS/FreedomStudio-3-1-1/SiFive\riscv-openocd-2.1.0\bin	openocd.exe	
Console X	(no launch history)			(h	o change it use the <u>global</u> or <u>workspace</u> preferences pages of 20 2222 Talout MMA TT KARA	a the project properties page)	
				Secure DM Key	This target does a	not have a secure Debug Module. No passkey is required.	
Build Cons	Debug As	> -		External auth command			Use default PKSD client script
LUFLAGS		1		JTAG Protocol J	TAG V (1) The BSP does not	I indicate what protocol to use. Choose wisely!	
./project	Debug Configurations	•		JTAG Connection J	TAG Probe 🗸 🕕 Connection is de	fined in the openood config script.	
:/project	Organiza Envoritor	•		OpenOCD Config Script	isp\openocd.cfg	 Project Work 	ospace File System Variables
LDLIBS=	organize Pavontes			Actual path 0	Oprojects\Customers\VLSISystemDesign\3.1.1\silive_hifive	1_sifive_welcome\bsp\openocd.cfg	Open in editor
FREERTOS ME	TAL VENV PATH="/C/project:	s/Cu		Config options:			A
_							
				Allocate console for Op	mOCD	Open telnet terminal	
				Remote Target			
				Host name or IP address:	localhost		
				Port number	3333		
							Restore defaul
		Filter matched 10 of 32 items					Reget Apply
		0					Debug Close

Figure 11: Alternate method to open debug session using OpenOCD

• You should see the debug window shown with 1 shown in Figure 12. To run the program, click on the "Run" button as represented by 2 in the same Figure 12

Sifve,	hifive1_sifive_welcom	e/src/sifive-welcome.c	- Freedom	Studio-3-1-1									0 ×
de Edit Surc	e Refactor <u>Navig</u>	ate Search Project	Bun SiF	FiveTools Window Help									
🔁 📲 🖓 🖬 🍋	0	- 🔄 - 🥭 🛷 -	10 0	🕨 🖩 🗱 🖎 🕫 Le 🗺 🕹 🖉 \$	s 😂 😂 🛛 🔂 🕘 👻 👻	ဆိုနှင့်တွင်ခုတ်နှံ 🛃 👘							Q 📝 😨
Project Expl er	×	🧙 🎖 🕀 🕴 = 🗖	Consol	le × 💽 Problems		🗟 🔊 🕑 😁 🖬 🕶 🗖 🕶	* Debug ×	Debugger Co	nsole 💊 E	Breakpoints		日 後一 ~	i 💀 🖇 🗖 🗖
Approx.120 ptr X Masses: I = 1 III Approx.120 ptr X Masses III IIII Approx.120 ptr X Bhares IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII			Freedom S monito symbo load I thread thread set m contin	<pre>Studio Message Console or reset init or halt 1-file 0:\projects\\sifive_hifive_hifi d apply all set \$pc_enter k main em inaccessible-by-default off nue</pre>	ve1_sifive_welcom ive_welcome\\src\	e\\src\\debug\\sifive-we \debug\\sifive-welcome.e	 ♥ sifive_hi ♥ sifive_hi ♥ sifive ♥ Ti ■ ■ a open ■ ■ ■ 	five1_sifive_welco -welcome.elf irread #1 (Suspen main() at sifive- occl.exe 54-unknown-elf-ç	ome_oper ided : Brea welcome.c gdb.exe	nocd [SiFive GDB Ope kpoint] :89 0x20101542	enOCD Debug Launch]		
LICENS	E.Apache2		Der	-						Pater la s		91 D	· · · · · ·
ILICENS	EMIT		g strive-v	weicome.c ×		L	Disassembl	y × 😹 Outline		Enter loca	auon nere 🔍 🛙 🖬 u		
In Makeri	le K and		81 1	metal_led_off(which_led);			20101540:	0×1000	addi	s0,sp,32	d got pab("ipa"	"nod") -	
in READN	ec.mo		82				20101542:	0x201007b7	lui	a5.0x20100	fection too ,	Teo /s	
> treatoms	metal		830 in	rt main (void)			20101540:	0x0dc78593	addi	a1,a5,1756 #	0x201006dc		1.1
> 😂 scripts > 🏶 Trace Com	npass		84 { 85 86 87	<pre>int rc; struct metal_led *led0_red, *</pre>	led0_green, *led0_	blue,	2010154a: 2010154e: 20101552: 20101556:	0x201007b7 0x6e078513 0x721000ef 0xfea42623	lui addi jal sw	a5,0x20100 a0,a5,1760 # ra,0x20102472 a0,-20(s0)	0x201006e0 <metal_led_get_r< td=""><td>gb></td><td></td></metal_led_get_r<>	gb>	
la freedom-e	e-sdk.mk		88	// This done will toggle LEDs	colone co un dofj	c them here	90		led0	_green = metal_	led_get_rgb("LD0"	, "green'	");
🗋 Makefile			89	<pre>led0_red = metal_led_get_rgb(</pre>	'LD0", "red");	-	2010155a:	0x201007b7	lui	a5.0x20100			
🗋 release.mi	k		90	<pre>led0_green = metal_led_get_rg led0_blue = metal_led_get_rg</pre>	("LD0", "green");				4				P
🖹 requireme	ints.txt		92	if ((led0 ced == NULL) (le	in green an NULL)	[] (led@ blue == NULL)	Trace View	er 🍠 Terminal 🗦	< 🖲 State	Browser	🚔 🖓 🕒 🕅 🔅) 🖍 🚮 🛛	0.8-0
sifive_hifiv	e1_sifive_welcomec	penocd.launch	93	printf("At least one of L	Ds is null.\n");		COM6	TCL:sifive_hifiv	e1_sifive_v	velcome_openocd :	×		
			94	return 1;			mhpmcounter	3 (/32): 0x0	0001234				
			95	}			mhpmevent3	(/32): 0x000	00000				
manufacture of 1991	Denist At Courses	B Marrier	96	// Eachla each LED			mhpmcounter	3h (/32): 0x	000000000)			
variable × ent	negist. In express.	Wenton	98	metal led enable(led0 red):			mpmcounter mpmcounter	(/32): 0x0 (/22): 0x0	0000000				
			99	metal led enable(led0 green);			mboncounter	4h (/32): 0x000	000000	9			
Name	type	value	100	<pre>metal_led_enable(led0_blue);</pre>			mhpmcounter	4 (/32): 0x0	0000000				
op rc	int	0x/statact	101				mcycleh (/3	 ex000000 	60				
> • ledu_red	struct metal_ied *	0x20100204	102	// All Off			mcycle (/32): 0x00d366f	7				
redu_green	struct metal_ied *	0x2010032a	103	metal_led_off(led0_red);			minstreth (/32): 0x0000	0000				
red0_blue	struct metal_led *	0x40006868	104	metal_led_off(led0_blue);			minstret (/	32): 0x003ta	900				
			106	accor_rco_orr(redo_brue),			mbpmcounter	3 (/32): 0x	000000000	,			
			107	// Lets get the CPU and its in	iterrupt		mhpmcounter	4h (/32): 0x	00000000)			
			108	cpu = metal_cpu_get(metal_cpu	_get_current_harti	d());	mhpmcounter	4 (/32): 0x0	0000000				1
							>						
Connected - Encodi	ing: windows, 1252												

Figure 12: Steps to run sifive-welcome program and observe output

• If you see a message "You have an active OpenOCD debug launch. Would you like to terminate that one and continue this one?" as shown in Figure 13, click on "Yes". Finally, you would see "SiFive" as output in the Com terminal represented by 2 in same Figure 13. The blue LED on VSDSquadron PRO should blink after this step.

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Figure 13: Run program and see output

3 Board Component Placement

The following figure shows the placement of various components on the VSDSquadron PRO RISC-V development board.

3.1 VSDSquadron PRO top view

The following Figure 14 shows the top view of the VSDSquadron PRO RISC-V development board.



Figure 14: Silkscreen Top View

3.2 VSDSquadron PRO bottom view

The following Figure 15 shows the bottom view of the VSDS quadron PRO RISC-V development board silkscreen.



Figure 15: Silkscreen Top View

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4 Revision History

The document's revision history provides a record of the alterations made to it, listed in chronological order, with the most recent revision first.

Revision	Date	Description
1.0	-	This is the first publica-
		tion of this document

Table 4: Revision History

5 Help and support

- Contact email ID vsd@vl
sisystemdesign.com
- Online Slack support https://vsdsquadron.slack.com/